In the Specification

Please delete the Paragraph beginning on Page 1, line 5 and replace it with the following Paragraph.

- -U.S. Patent Application No. 10/728,627 ~~(TI-34654)~~, entitled APPARATUS AND METHOD FOR SYNCHRONIZATION OF TRACE STREAMS FROM MULTIPLE PROCESSORS, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,212 ~~(TI-34655)~~, entitled APPARATUS AND METHOD FOR SEPARATING DETECTION AND ASSERTION OF A TRIGGER EVENT, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,239 ~~(TI-34656)~~, entitled APPARATUS AND METHOD FOR STATE SELECTABLE TRACE STREAM GENERATION, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,650 ~~(TI-34657)~~, entitled APPARATUS AND METHOD FOR SELECTING PROGRAM HALTS IN AN UNPROTECTED PIPELINE AT NON-INTERRUPTIBLE POINTS IN CODE EXECUTION, invented by Gary L. Swoboda and Krishna Allam, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,591 ~~(TI-34658)~~, entitled APPARATUS AND METHOD FOR REPORTING PROGRAM HALTS IN AN UNPROTECTED PIPELINE AT NON-INTERRUPTIBLE POINTS IN CODE EXECUTION, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present

application; U.S. Patent Application No. 10/729,407 ~~(TI-34659)~~, entitled APPARATUS AND METHOD FOR A FLUSH PROCEDURE IN AN INTERRUPTED TRACE STREAM, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,564 ~~(TI-34660)~~, entitled APPARATUS AND METHOD FOR CAPTURING AN EVENT OR COMBINATION OF EVENTS RESULTING IN A TRIGGER SIGNAL IN A TARGET PROCESSOR, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,400 ~~(TI-34661)~~, entitled APPARATUS AND METHOD FOR CAPTURING THE PROGRAM COUNTER ADDRESS ASSOCIATED WITH A TRIGGER SIGNAL IN A TARGET PROCESSOR, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,639 ~~(TI-34663)~~, entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PROCESSOR RESET, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent No. 10/729,214 ~~(TI-34664)~~, entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PROCESSOR DEBUG HALT SIGNAL, invented by Gary L. Swoboda, Bryan Thome, Lewis Nardini and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,327 ~~(TI-34665)~~, entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PIPELINE FLATTENER PRIMARY CODE FLUSH FOLLOWING INITIATION OF AN INTERRUPT SERVICE ROUTINE; invented by Gary L. Swoboda,

Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,647 ~~(TI-34666)~~, entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PIPELINE FLATTENER SECONDARY CODE FLUSH FOLLOWING A RETURN TO PRIMARY CODE EXECUTION, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,401 ~~(TI-34667)~~, entitled APPARATUS AND METHOD IDENTIFICATION OF A PRIMARY CODE START SYNC POINT FOLLOWING A RETURN TO PRIMARY CODE EXECUTION, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U. S. Patent Application No. 10/729,326 ~~(TI-34668)~~, entitled APPARATUS AND METHOD FOR IDENTIFICATION OF A NEW SECONDARY CODE START POINT FOLLOWING A RETURN FROM A SECONDARY CODE EXECUTION, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,190 ~~(TI-34669)~~, entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PAUSE POINT IN A CODE EXECTION SEQUENCE, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application No. 10/729,196 ~~(TI-34670)~~, entitled APPARATUS AND METHOD FOR COMPRESSION OF A TIMING TRACE STREAM, invented by Gary L. Swoboda and Bryan Thome, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent

Application No. 10/729,272 ~~(TI-34671)~~, entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFCATION OF MULTIPLE TARGET PROCESSOR EVENTS, invented by Gary L. Swoboda and Bryan Thome, filed on even date herewith, and assigned to the assignee of the present application; and U.S. Patent Application No. 10/729,191 ~~(TI-34672)~~ entitled APPARATUS AND METHOD FOR OP CODE EXTENSION IN PACKET GROUPS TRANSMITTED IN TRACE STREAMS, invented by Gary L. Swoboda and Bryan Thome, filed on even date herewith, and assigned to the assignee of the present application are related applications.- -

Please delete the Paragraph beginning on Page 18, line 9 of the specification and replace that Paragraph with the following Paragraph.

- - The comparator of the present invention is particularly useful in the test and debug procedures of a target processor. In analyzing the operation of target processing system, it is important to know the events that result in the change in operation produced by a trigger signal. The present invention captures an identification of the events that result in the change in operation, e.g., the transition to an interrupt service routine. These events are captured only in the event that an actual trigger signal is generated. Upon the generation of a trigger signal, signals specifying the events causing the trigger signal are stored and can be transferred to the host processing unit for analysis. In addition, it is

necessary to determine where in the program execution the trigger signal occurred as well as the events that resulted in the generation of the trigger signal. The contents of the program counter are the best indication of the state of program execution at the time of the trigger signal. However, because of the pipeline delay (and, if present, a pipeline flattener delay), the events that result in the generation of the trigger signal are the result of instructions that began execution before the delay. Consequently, in order to correlate the events causing the trigger signal with the appropriate instruction identified by the program counter, ~~the~~ a delay is added in the instruction applied to the register. In this manner, the target processor events resulting in the generation of a trigger signal and the related position in the instruction execution can be identified and transferred to the host processing unit for analysis. In the preferred embodiment shown in Fig. 2 and Fig. 3, bus A and bus B are both coupled to the addresses referenced by the program counter. The comparator unit is then used to generate an EVENT signal that is applied to the trigger unit. However, the comparator of the present ~~has~~ invention has wider application. For example, two addresses can be applied to the comparator on the two buses and analyzed separately. ~~For example, a program counter address and an address referenced by the program counter address can be analyzed separately.~~ - -